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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/430,366	10/28/1999	MARK T. RAMSBEY	0180164	7206

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EXAMINER	
CHEN, JACK S J	

ART UNIT	PAPER NUMBER
2813	

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31

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/430,366	RAMSBEY ET AL.
	Examiner	Art Unit
	Jack Chen	2813

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 August 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4,5,7,9-11,14,15 and 23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4,5,7,9-11,14,15 and 23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

In response to the communication filed on August 20, 2003, claims 1, 4-5, 7, 9-11, 14-15 and 23 are active in this application.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1, 4-5, 7, 9-11, 14-15 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamagishi et al., U.S./5,808,339 taken with Sze et al., "ULSI Technology" or Paterson et al., U.S./4,613,956 and in view of Applicant's admitted prior art.

Yamagishi et al. (figs. 9A- 10D) discloses a method for forming; a semiconductor device having a substrate 11 and a tunnel oxide 51 (fig. 9C; NOTE: the oxide layer 51 is formed across

the substrate, which includes the element isolation region) formed on the substrate, which comprises depositing a floating gate layer 53 on the tunnel oxide to a first thickness; etching the floating gate layer to provide a floating gate 53; depositing an insulator layer of oxide 54 by CVD METHOD (fig. 9E, col. 12, lines 27-31, which inherently shows the CVD oxide is the high temperature/quality oxide; further in this regard, it should be noted that LPCVD is a type of CVD process. Moreover, on page 4, lines 27-29 of the instant application, applicant discloses that any other dielectric material will provide the same results and the disclosure fails to mention the criticality of the LPCVD process) directly on exposed portions of the tunnel oxide layer (it should be noted that layer 51 is formed on the substrate as well as the isolation region, see figs. 9B-9C) and the floating gate (Yamagishi et al. inherently shows the insulator prevents charge leaking from the floating gate since it seals the floating gate); wherein the insulator layer has a second thickness that is greater than the first thickness (fig. 9E), wherein the insulator layer is in contact with vertical surfaces of the floating gate (fig. 9E); polishing (i.e., CMP) the insulator layer immediately after the step of depositing the insulator layer to provide a planar surface that exposes a top surface of the floating gate and the insulator layer (fig. 10A); depositing a dielectric layer 55 (ONO. fig. 10B, col. 12, lines 57-67) on the planar surface directly over the exposed top surface of the floating gate and the insulator layer; depositing a control gate layer 56 (fig. 10B) on the ONO layer; and etching the control gate layer and the ONO layer to form a stacked gate structure of the flash memory cell (fig. 10D). See figs. 1-12B and cols. 1-16 for more details.

However; Yamagishi et al. is silent to forming high temperature oxide by using *LPCVD* method (Note: during the telephone interview dated on 8/3/2001. Applicant admitted that the

process for forming this layer by using LPCVD method is well known in the art, also see the amendment dated on 8/6/2001; furthermore, applicant stated in the specification, other dielectric may used, i.e., see page 3, lines 26-30. In addition, the disclosure fails to mention the criticality of the LPCVD process).

It is well known in the art to form the dielectric by using any CVD process. For example, Sze et al. teaches forming the dielectric by using I.PCVD process, such will provide excellent purity and uniformity, conformal step coverage, large wafer capacity and high throughput, etc. Furthermore, it is well known in the art to use doped polysilicon or doped amorphous silicon for the floating gate, such will increase the conductivity of the floating gate. For example, applicant's admitted prior art teaches using doped polysilicon or doped amorphous silicon for the floating gate, see pages 1-2. Paterson et al. also discloses a method for forming a semiconductor device, which includes depositing the high temperature/quality oxide on the floating gate by LPCVD in order to provide high uniformity and a highly doped floating pate (col. 3, lines 65-col. 4, lines 6 and col. 4. line 67-col. 5, line 47) and using ONO for the inter-poly dielectric, see figs. 1-8c, cols. 1-10 for more details.

Therefore, the subject matter as a whole would have been obvious to one having ordinary skill in the art at the time the invention was made to use LPCVD oxide as taught by Sze et al. or Paterson et al. in the method of Yamagishi et al. in order to provide excellent purity and uniformity, conformal step coverage, large wafer capacity and high throughput. And using doped polysilicon or amorphous silicon for the floating gate as taught by applicant's admitted prior art in the method of Yamagishi et al. in order to increase the conductivity of the floating gate. Furthermore, it would have been obvious to one having ordinary skill in the art at the time

the invention was made to modify the method of Yamagishi et al. by selecting the suitable thicknesses for the floating gate and the insulator layer, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

4. Claims 1, 4-5, 7, 9-11 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu, U.S./6,033,956 or Mitchell et al., U.S./4,713,142 taken with Yamagishi et al., U.S./5,808,339 and in view of Sze et al., "ULSI Technology" or Paterson et al., U.S./4,613,956.

Wu discloses a method for forming a semiconductor device having a substrate and a tunnel oxide 202 formed on the substrate (fig. 2A), which comprises depositing a floating gate layer on the tunnel oxide to a first thickness; etching the floating gate layer, to provide a floating gate 204 (fig. 2A); depositing an insulator layer of oxide 210 (CVD oxide. inherently shows the oxide is the high temperature oxide and not limited to any particular type CVD methods [i.e.. LPCVD, PECVD, etc.], which produces the high temperature/duality oxide; furthermore, on page 4, lines 27-29 of the instant application, applicant discloses that any other dielectric material will provide the same results. In addition, the disclosure fails to mention the criticality of the I.PCVD process) directly on exposed portions of the tunnel oxide and the floating gate such that the insulator layer has a second thickness that is greater than the first thickness (inherently shows using the insulator layer to prevent charge leaking from the floating gate. see fig. 2C), wherein the insulator layer 210 is in contact with vertical surfaces of the floating gate; polishing the insulator layer to provide a planar surface that exposes a top surface of the floating gate and the insulator layer (fig. 2c); and depositing a dielectric layer 214 (note: in an alternate

embodiment. ONO is used, see col. 3, lines 24-31) on the planar surface directly over the exposed top surface of the floating gate and the insulator layer, see figs. 1-4G and cols. 1-6 for more details.

Mitchell et al. also disclose a method for forming a semiconductor device having a substrate and a tunnel oxide 32 (fig. 2a) formed on the substrate, which comprises depositing a floating gate layer on the tunnel oxide to a first thickness; etching the floating gate layer, to provide a floating gate 33 (fig. 2a); depositing an insulator layer (***note: both layers 36 and 37 can be considered as an insulating layer***) of oxide 36 and 37 (CVD oxide, inherently shows the oxide is the high temperature oxide and is not limited to any particular type CVD methods [i.e.. I.PCVD, PECVD, etc.], which produces the high temperature/quality oxide; furthermore, on page 4, lines 27-29 of the instant application, applicant discloses that any other dielectric material will provide the same results. In addition, the disclosure fails to mention the criticality of the LPCVD process) directly on exposed portions of the tunnel oxide and the floating gate such that the insulator layer has a thickness that is greater than the first thickness (fig. 2c), wherein the insulator layer 36/37 is in contact with vertical surfaces of the floating gate to prevent charge leaking from the floating gate; polishing the insulator layer to provide a planar surface that exposes a top surface of the floating gate and the insulator layer (fig. 2d): and depositing a dielectric layer 39 on the planar surface directly over the exposed top surface of the floating gate and the insulator layer. See figs. 1-5 and cols. 1-6 for more details.

However; Wu and Mitchell et al. are silent to forming high temperature oxide by using *LPCVD* method (Note: during the telephone interview dated on 8/3/2001. Applicant admitted that the process for forming this layer by using LPCVD method is well known in the art, also see

the amendment dated on 8/6/2001; furthermore, applicant stated in the specification, other dielectric may used, i.e., see page 3, lines 26-30. In addition, the disclosure fails to mention the criticality of the LPCVD process).

It is well known in the art to form the dielectric by using any CVD process. For example, Sze et al. teaches forming the dielectric by using I.PCVD process, such will provide excellent purity and uniformity, conformal step coverage, large wafer capacity and high throughput, etc. Paterson et al. also discloses a method for forming a semiconductor device, which includes depositing the high temperature/quality oxide on the floating gate by LPCVD in order to provide high uniformity and a highly doped floating pate (col. 3, lines 65-col. 4, lines 6 and col. 4. line 67-col. 5, line 47) and using ONO for the inter-poly dielectric, see figs. 1-8c, cols. 1-10 for more details.

Therefore, the subject matter as a whole would have been obvious to one having ordinary skill in the art at the time the invention was made to use LPCVD oxide as taught by Sze et al. or Paterson et al. in the method of Wu or Mitchell et al. in order to provide excellent purity and uniformity, conformal step coverage, large wafer capacity and high throughput and using ONO layer as the inter-poly dielectric as taught by Paterson et al. in the method of Wu or Mitchell et al. in order to provide high capacitance. Furthermore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method of Wu or Mitchell et al. by selecting the suitable thicknesses for the floating gate and the insulator layer, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

The further differences between the instant claims (1, 7 and 23) and the prior art (Wu; Mitchell et al.; Paterson et al. and Sze et al.) are as following: Wu, Mitchell et al., Paterson et al. and Sze et al. disclosed above. However, these references are silent to polishing the insulator layer immediately after the step of depositing the insulator layer.

Yamagishi et al. (figs. 9A- l0D) discloses a method for forming; a semiconductor device having a substrate 11 and a tunnel oxide 51 (fig. 9C; NOTE: the oxide layer 51 is formed across the substrate, which includes the element isolation region) formed on the substrate, which comprises depositing a floating gate layer 53 on the tunnel oxide to a first thickness; etching the floating gate layer to provide a floating gate 53; depositing an insulator layer of oxide 54 by CVD METHOD (fig. 9E, col. 12, lines 27-31, which inherently shows the CVD oxide is the high temperature/quality oxide; further in this regard, it should be noted that LPCVD is a type of CVD process. Moreover, on page 4, lines 27-29 of the instant application, applicant discloses that any other dielectric material will provide the same results and the disclosure fails to mention the criticality of the LPCVD process) directly on exposed portions of the tunnel oxide layer (it should be noted that layer 51 is formed on the substrate as well as the isolation region, see figs. 9B-9C) and the floating gate (Yamagishi et al. inherently shows the insulator prevents charge leaking from the floating gate since it seals the floating gate); wherein the insulator layer has a second thickness that is greater than the first thickness (fig. 9E), wherein the insulator layer is in contact with vertical surfaces of the floating gate (fig. 9E); ***polishing (i.e., CMP) the insulator layer immediately after the step of depositing the insulator layer to provide a planar surface that exposes a top surface of the floating gate and the insulator layer (fig. l 0A);*** depositing a dielectric layer 55 (ONO. fig. 10B, col. 12, lines 57-67) on the planar surface directly over the

exposed top surface of the floating gate and the insulator layer; depositing a control gate layer 56 (fig. 10B) on the ONO layer; and etching the control gate layer and the ONO layer to form a stacked gate structure of the flash memory cell (fig. 10D). See figs. 1-12B and cols. 1-16 for more details.

Therefore, the subject matter as a whole would have been obvious to one having ordinary skill in the art at the time the invention was made to use CMP method right after depositing the insulator as taught by Yamagishi et al. in the method of Wu or Mitchell et al. in order to simplify the overall processes and provide a planar surface. Furthermore, using either CMP or back etching method is Art Recognized equivalent, one of ordinary skill in the art would have found it obvious to substitute one for another.

5. Claims 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu, U.S./6,033,956 or Mitchell et al., U.S./4,713,142 taken with Yamagishi et al., U.S./5,808,339 and in view of Sze et al., "ULSI Technology" or Paterson et al., U.S./4,613,956 as applied to claims 1, 4-5, 7, 9-11 and 23 above, and further in view of Applicant's admitted prior art.

The further differences between the instant claims 14-15 and the prior art are as following: Wu and Mitchell et al. disclosed above. However. Wu and Mitchell et al. are silent to use doped polysilicon or amorphous silicon for the floating gate. Applicant's admitted prior art teaches using doped polysilicon or doped amorphous silicon for the floating gate, see pages 1-2.

Therefore, the subject matter as a whole would have been obvious to one laving ordinary skill in the art at the time the invention was made to use doped polysilicon or amorphous silicon

for the floating gate as taught by applicant's admitted prior art in the method of Wu or Mitchell et al. in order to increase the conductivity of the floating gate.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jack Chen whose telephone number is (703)308-5838. The examiner can normally be reached on Monday-Friday (8:30am-6:00pm) alternate Monday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W Whitehead can be reached on (703)308-4940. The fax phone number for the organization where this application or proceeding is assigned is (703)872-9318.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Jack Chen
Primary Examiner
Art Unit 2813